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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.	
09/840,600	04/23/2001	Roger S. Tsai	12-1120	3792	
75	590 07/01/2003				
•	Patent, Counsel			EXAMINER	
TRW, Inc. Law Department TRAN, THI				HIEN F	
	k, Building E2/6051		ART UNIT	PAPER NUMBER	
Redondo Beach	1, CA 90278		2811		
			DATE MAILED: 07/01/2003		

Please find below and/or attached an Office communication concerning this application or proceeding.

,	Application No.	Applicant(s)	Um
	09/840,600	TSAI, ROGER S.	
Office Action Summ ry	Examiner	Art Unit	
	Thien Tran	2811	
The MAILING DATE of this communication Period for Reply	appears on the cover sheet w	ith the correspondence address -	-
A SHORTENED STATUTORY PERIOD FOR RE THE MAILING DATE OF THIS COMMUNICATIO - Extensions of time may be available under the provisions of 37 CFI after SIX (6) MONTHS from the mailing date of this communication - If the period for reply specified above, the maximum statutory pe - Failure to reply within the set or extended period for reply will, by st - Any reply received by the Office later than three months after the m earned patent term adjustment. See 37 CFR 1.704(b). Status	ON. R 1.136(a). In no event, however, may a in. In reply within the statutory minimum of thire in apply and will expire SIX (6) MON latute, cause the application to become Al	reply be timely filed ty (30) days will be considered timely. ITHS from the mailing date of this communica BANDONED (35 U.S.C. § 133).	ition.
1) Responsive to communication(s) filed on			
2a)⊠ This action is FINAL . 2b)□	This action is non-final.		
3) Since this application is in condition for all closed in accordance with the practice uncondition of Claims	lowance except for formal ma der <i>Ex parte Quayle</i> , 1935 C.	tters, prosecution as to the meri D. 11, 453 O.G. 213.	ts is
Disposition of Claims 4)⊠ Claim(s) 1 and 4-19 is/are pending in the a	annlication		
4a) Of the above claim(s) is/are with			
5)⊠ Claim(s) <u>13-15</u> is/are allowed.			
6)⊠ Claim(s) <u>1,5-12,16,18 and 19</u> is/are rejecte	ed.		
7)⊠ Claim(s) <u>4 and 17</u> is/are objected to.			
8) Claim(s) are subject to restriction ar	nd/or election requirement.		
Application Papers	·		
9)☐ The specification is objected to by the Exam	niner.		
10)☐ The drawing(s) filed on is/are: a)☐ a	ccepted or b) objected to by t	the Examiner.	
Applicant may not request that any objection t			
11) The proposed drawing correction filed on	is: a)□ approved b)□ c	lisapproved by the Examiner.	
If approved, corrected drawings are required in			
12)☐ The oath or declaration is objected to by the	Examiner.		
Priority under 35 U.S.C. §§ 119 and 120			
13) Acknowledgment is made of a claim for for	reign priority under 35 U.S.C.	§ 119(a)-(d) or (f).	
a) ☐ All b) ☐ Some * c) ☐ None of:			
1. Certified copies of the priority docum			
2. Certified copies of the priority docum	nents have been received in A	Application No	
3. Copies of the certified copies of the application from the Internationa * See the attached detailed Office action for a	l Bureau (PCT Rule 17.2(a)).		
14)☐ Acknowledgment is made of a claim for dom	nestic priority under 35 U.S.C.	§ 119(e) (to a provisional applic	ation).
a) The translation of the foreign language	-		
Attachment(s)	•		
1) Notice of References Cited (PTO-892) 2) Notice of Draftsperson's Patent Drawing Review (PTO-948) 3) Information Disclosure Statement(s) (PTO-1449) Paper Notice) 5) Notice of	Summary (PTO-413) Paper No(s) Informal Patent Application (PTO-152)	

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DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 6-7 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 6-7 recite the limitation "step (d)" in line 1. There is insufficient antecedent basis for this limitation in the claims.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 5-7, 16, 18 and 19 are rejected under 35 U.S.C. 102(b) as being anticipated by Mahon et al. ("A Technique for Modelling S-Parameters for HEMT Structures as a Function of Gate Bias", IEEE Transactions on Microwave Theory and Techniques, Vol. 40, No.7, July 1992).

Mahon et al. disclose the claimed method of modeling a semiconductor device comprising the steps of modeling a small signal electrical equivalent circuit (Fig. 1) for the semiconductor device (HEMT device) which includes a plurality of electrical circuit elements defining a small signal model, said small signal equivalent circuit based in part

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on physical gate length and wafer structure such as doping densities which the examiner characterizes as real process parameters; and deriving the electrical circuit elements at least in part from a small signal excitation analysis of at least electrical field characteristics of the semiconductor device (see pages 1431 and 1433).

Regarding claim 5, Mahon further discloses the step of determining the relationships between conduction band and electrical permitivities and the material composition for the materials in the semiconductor device (see page 1431).

Regarding claim 6, Mahon et al. discloses analytically determining the relationships between the electrical permitivity, conduction band and material composition.

Regarding claim 7, Mahon et al. further discloses the step of fitting simulated data.

Regarding claim 16, said semiconductor device model is based at least in part as a function of one or more of conduction band offsets; electrical permitivities; and material composition of the wafer structure.

Regarding claim 18, said semiconductor device is a HEMT.

Regarding claim 19, said semiconductor device is a FET.

Claims 8-12 rejected under 35 U.S.C. 103(a) as being unpatentable over Mahon et al. in view of Hirose et al. (A Possible Scaling Limit for Enhancement-Mode GaAs MESFET's in DCFL Circuits", IEEE Transactions on Electron Devices, Vol. 39, No. 12, Dec. 1992).

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Mahon et al. as described above does not specifically disclose determining the electron transport characteristics of any bulk materials in the semiconductor, determining the undepleted linear channel mobility by material characterization or physical simulation, and determining the schottky barrier height expressions. However, such determinations are known in the art for modeling HEMT device as disclosed for example by Hirose et al. (sections II and III). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to further include the steps of determining the electron transport characteristics of any bulk materials in the semiconductor, determining the undepleted linear channel mobility by material characterization or physical simulation, and determining the schottky barrier height expressions as taught by Hirose et al. into the method of Mahon et al. in order to achieve higher speeds.

Allowable Subject Matter

Claims 13-15 are allowed.

Claims 4, 17 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: Prior art references do not teach or render obvious a method of modeling a semiconductor device wherein real process parameters include at least one of gate length recess, etch depth, recess undercut dimensions and passivation nitrite thickness.

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Prior art references do not teach or render obvious a method of modeling a semiconductor device comprising the steps of forming semiconductor physical equations with empirical terms for modeling one or more of the following characteristics fundamental charge control physics for sheet charge in an active channel as controlled by a gate terminal voltage; average centroid position of the sheet charge within the active channel width; position of charge partitioning boundaries as a function of gate, drain and source terminal voltages; bias dependence of linear channel mobility and surface depleted regions; bias dependence of a velocity saturating electric field of the channel; saturated electron velocity; electrical conductance within the linear region of the channel, under the gate; electrical conductance within the source and drain access regions.

Response to Arguments

Applicant's arguments with respect to claims 1, 5-12, 16 and 18-19 have been considered but are most in view of the new ground(s) of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not

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mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

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Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thien Tran whose telephone number is (703) 308-4108. The examiner can normally be reached on 8:30AM - 5:00PM Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (703) 308-2772. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9318 for regular communications and (703) 872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

tt June 26, 2003

Thien Tran
Patent Examiner
Technology Center 2800